

CS 371 Test plan for register file

FSEL	BinSel	input					output		Rational
		Asel	Bsel	WSel	Wenable	Value	R0	R1	
PassB	value	X	X	0	0	A	R0	R1	no change with write enable = 0
PassB	value	X	X	1	0	A	R0	R1	no change with write enable = 0
PassB	value	X	X	0	1	A	A	R1	simple write to R0
PassB	value	X	X	0	1	5	5	R1	simple write to R0 (other bits)
PassB	value	X	X	1	1	F	R0	F	simple write to R1
PassB	value	X	X	1	1	0	R0	0	simple write to R1
PassB	value	X	X	1	1	0	R0	0	simple write to R1
PassB	value	X	X	1	1	3	R0	3	cycle through test
Add	reg	1	1	1	1	X	R0	6	source select 1
PassB	reg	X	1	0	1	X	6	6	transfer value from R1 to R0
PassB	value	X	X	1	1	7	R0	7	setup
PassB	reg	X	0	1	1	X	7	7	transfer value from R0 to R1
Add	reg	0	0	1	1	X	7	E	source select 0 test