Goal: Speed up address translation with paging, OR waste less memory with paging

**Issue 1 – Paging is sloooow**

New algorithm:

1. Get Virtual Page Number (VPN) from virtual address
2. If TLB Hit
   a. Extract page frame number (PFN) from TLB entry to get physical address
3. [start at same time as 2] (in case of TLB Miss)
   a. `Access PT`
   b. `Update TLB`

Example:

```
int sum = 0;
for(i = 0; i < 10; i++)
    sum += a[i];  //assume a is an array
```

Principles of Caching:

- **Locality**
- **Spaced**
- **Temporal**

Context switches are even more costly now
Issue 2 – Page Tables are Big

Easy solution: make the page table more modular

Better Solution: page the page table

Core concept: space time trade off

But Recall: TLB high hit rate